20 and 21, and amends the specification to accommodate these proposed drawing changes.

Applicant will proceed to submit formal revisions to the drawings upon approval of the proposed red-line changes and allowance of the present application. With approval of these changes, Applicant respectfully requests that the Examiner withdraw the objection to the drawing.

OBJECTED CLAIMS

Claims 2 – 8, 10 – 13, 18, 19 and 24 are objected to as being dependent on rejected base claim 1. Applicant amends claims 2, 3 and 11 to include the limitations of claim 1, respectfully submits that claims 2, 3 and 11 are thereby allowable, and requests that this objection be withdrawn with respect to claims 2, 3 and 11. As claims 4 – 8, 10, 12-13, 18, 19 and 24 depend either directly or indirectly from allowable claim 3, Applicant further submits that these claims are allowable, and requests that the objection be withdrawn with respect to claims 4 – 8, 10, 12-13, 18, 19 and 24.

CLAIM REJECTION UNDER 35 U.S.C. § 103(a)

Claim 1 is rejected under 35 U.S.C. §102(e) as being anticipated by Japanese Patent Publication 2000-100955 to Kazuo. Applicant respectfully traverses the rejection under 35 U.S.C. §102(e).

In claim 1, Applicant discloses a flip-chip semiconductor device having a multi-layered structure including a cell forming layer and a pad forming layer. The device includes input and output cells and macro-cells formed in the cell-forming layer, power supply pads formed in the pad forming layer that are electrically connected to the input and output cells, and signal pads formed in the pad forming layer that are electrically connected to the input and output cells.

Importantly, the signal pads are arranged in a peripheral area outside of the area of the power supply pads (see, e.g., page 9, line 15 through page 13, line 3 of Applicant's specification). For example, the signal pads 31/32/33 are outside of the power supply pads 11/12 in the first embodiment shown in Fig. 3.

This feature is desirable, because the semiconductor structure becomes simple. If the signal pads are mixed with the power supply pads as those in the admitted prior art, the manufacturing process changes the signal lines from the upper level to a lower level and vice versa due to the adjacent power supply pads. As a result of the inventive configuration, however, power and signal lines may be routed in the peripheral area without via holes and added layers for routing power lines around signal lines. Thus, if the signal pads and power supply pads are arranged as claimed, the signal lines are routed in a simple manner.

Kazuo discloses a semiconductor integrated circuit device having a plurality of input and output cells arranged at the periphery of an LSI chip, and featuring a common pullout pattern repeatably used for wiring cells to pads. However, Kazuo is silent as to how pads 5 are assigned to supply signal and power to input and output cells 2. In

particular, Kazuo fails to disclose or otherwise suggest Applicant's configuration in which input and output signal pads are located above the peripheral area defined by the input and output cells, and the input and output signal pads located above the peripheral area defined by the input and output cells are arranged outside of the area of the power supply pads. For example, Fig 3 of Kazuo appears to illustrate a signal pad 15 located outside of the area defined by the input and output cells.

Accordingly, Applicant respectfully submits that claim 1 is not anticipated by Kazuo, and is therefore in condition for allowance.

CONCLUSION

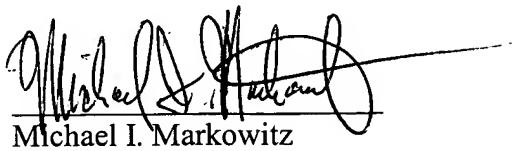
An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that claims 1-8, 10-13, 18, 19 and 24, comprising independent claims 1, 2, 3, and 11 and the claims that depend therefrom, are in condition for allowance. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Attached is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned **"Version With Marks To Show Changes Made".**

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,



Michael I. Markowitz
Reg. No. 30,659

Enclosure: Version With Markings To Show Changes Made
Amended Figs. 3 and 6
New Figs. 20 and 21

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VERSION WITH MARKINGS TO SHOW CHANGES MADE – S/N 10/024,154

IN THE SPECIFICATION

Please amend the paragraph beginning at page 7, line 21 as follows:

Fig. 18 is a plane view showing the layout of pads and input and output cells for several modifications; [and]

Please insert the following paragraphs following page 7, line 23:

Fig. 20 is a cross-sectional view of the flip-chip semiconductor device of Fig. 3; and

Fig. 21 is a plane view showing a portion of a layout of a flip-chip semiconductor device consistent with the principles of the device of Fig. 3.

Please amend the paragraph beginning at page 8, line 13 as follows:

Most of the peripheral area 1b is assigned to input and output circuits such as those labeled with 21/ 22/ 23 and signal pads such as those labeled with 31/ 32/ 33. The input and output cells are herein below referred to as "input and output cells", and the signal pads are electrically connected to the input and output cells. Each of the input and output cells is implemented by an output driver circuit and/ or input buffer circuit. An input and output controlling circuit may be further incorporated in the input and output cell. An input and output control circuit may be further incorporated in the input and output cell. Although the input and output cells are drawn on a level with the signal pads in figures 3 and 4, the flip chip semiconductor device has a multi- layered structure, and the input and output cells are assigned a certain level lower than the level assigned to the

signal pads. This assigned level may be referred to as a "cell forming layer." The signal pads are formed on the highest level of the multi- layered structure. The highest level is herein below referred to as "pad forming layer". Figure 20 presents a cross-sectional view through the flip-chip semiconductor device 1 of Figure 3, illustrating cell forming layer 1e, pad forming layer 1g, and intermediate layers 1f.

Please amend the paragraph beginning at page 11, line 21 as follows:

The inner area of the pad forming layer is assigned to power supply pads 13/ 14. The power supply pads 13 are assigned to the power voltage VDD, and the power supply pads 14 are assigned to the other power voltage VSS. The power supply pads 13 are represented by small squares in figure 3, and each of the power supply pads 13 is hatched with oblique lines drawn from the upper corner of the left side to the lower corner of the right side. The power supply pads 14 are also represented by small squares. However, each of the power supply pads 14 is hatched with oblique lines drawn from the upper corner of the right side to the lower corner of the left side. Thus, the potential level on the power supply pads 13/ 14 is discriminated by comparing the direction of the hatching lines. As will be seen in figure 3, the power supply pads 13 are arranged in staggered fashion. On the other hand, the other power supply pads 14 occupy the vacant areas among the power supply pads 13, and are also laid on a staggered pattern. Macro-cells such as logic cells are fabricated under the inner area on the pad forming layer, and the power voltages VSS and VDD are supplied from the power supply pads 13/ 14 to the logic cells through via-holes. However, the input and output cells do not perfectly

occupy the peripheral area 1b of the certain level. In other words, there [is] are vacancies among the regions assigned to the input and output cells in the peripheral area 1b on the certain level. The manufacturer can assign other macro-cells to the vacancies (for example, as illustrated in Figure 21 by macro-cell 24 positioned in a vacancy in peripheral area 1b of device 1). Thus, any real estate is not wasted.

IN THE CLAIMS

Please amend claims 1, 2, 3, and 11 as follows:

1. (Amended) A flip chip semiconductor device of a multiplexing-layered structure having a cell forming layer and a pad forming layer, comprising:

input and output cells formed in said cell forming layer together with macro-cells;

power supply pads formed in said pad forming layer, and electrically connected to said input and output cells; and

signal pads formed in said pad forming layer, electrically connected to said input and output cells, and arranged in an area outside of an area of said power supply pads.

2. (Amended) A flip chip semiconductor device of a multi-layered structure having a cell forming layer and a pad forming layer, comprising:

input and output cells formed in said cell forming layer together with macro-cells;

power supply pads formed in said pad forming layer, and electrically connected to said input and output cells; and

signal pads formed in said pad forming layer, electrically connected to said input and output cells, and arranged outside of said power supply pads;

[The flip chip semiconductor device as set forth in claim 1,] in which said signal pads and said power supply pads are to be connected to corresponding signal pads directly connected to signal lines without passing through a different layer and corresponding power supply pads formed on a pad forming layer of a multi-layered package substrate.

3. (Amended) A flip chip semiconductor device of a multi-layered structure having a cell forming layer and a pad forming layer, comprising:

input and output cells formed in said cell forming layer together with macro-cells;

power supply pads formed in said pad forming layer, and electrically connected to said input and output cells; and

signal pads formed in said pad forming layer, electrically connected to said input and output cells, and arranged outside of said power supply pads;

[The flip chip semiconductor device as set forth in claim 1,] in which said input and output cells form input and output cell groups which in turn form columns of input and output cell groups extending in directions crossing peripheral edges of said pad forming layer.

11. (Amended) A flip chip semiconductor device of a multi-layered structure having a cell forming layer and a pad forming layer, comprising:

input and output cells formed in said cell forming layer together with macro-cells;

power supply pads formed in said pad forming layer, and electrically connected to said input and output cells; and

signal pads formed in said pad forming layer, electrically connected to said input and output cells, and arranged outside of said power supply pads;

[The flip chip semiconductor device as set forth in claim 1,] in which said macro-cells are formed inside of said input and output cells.

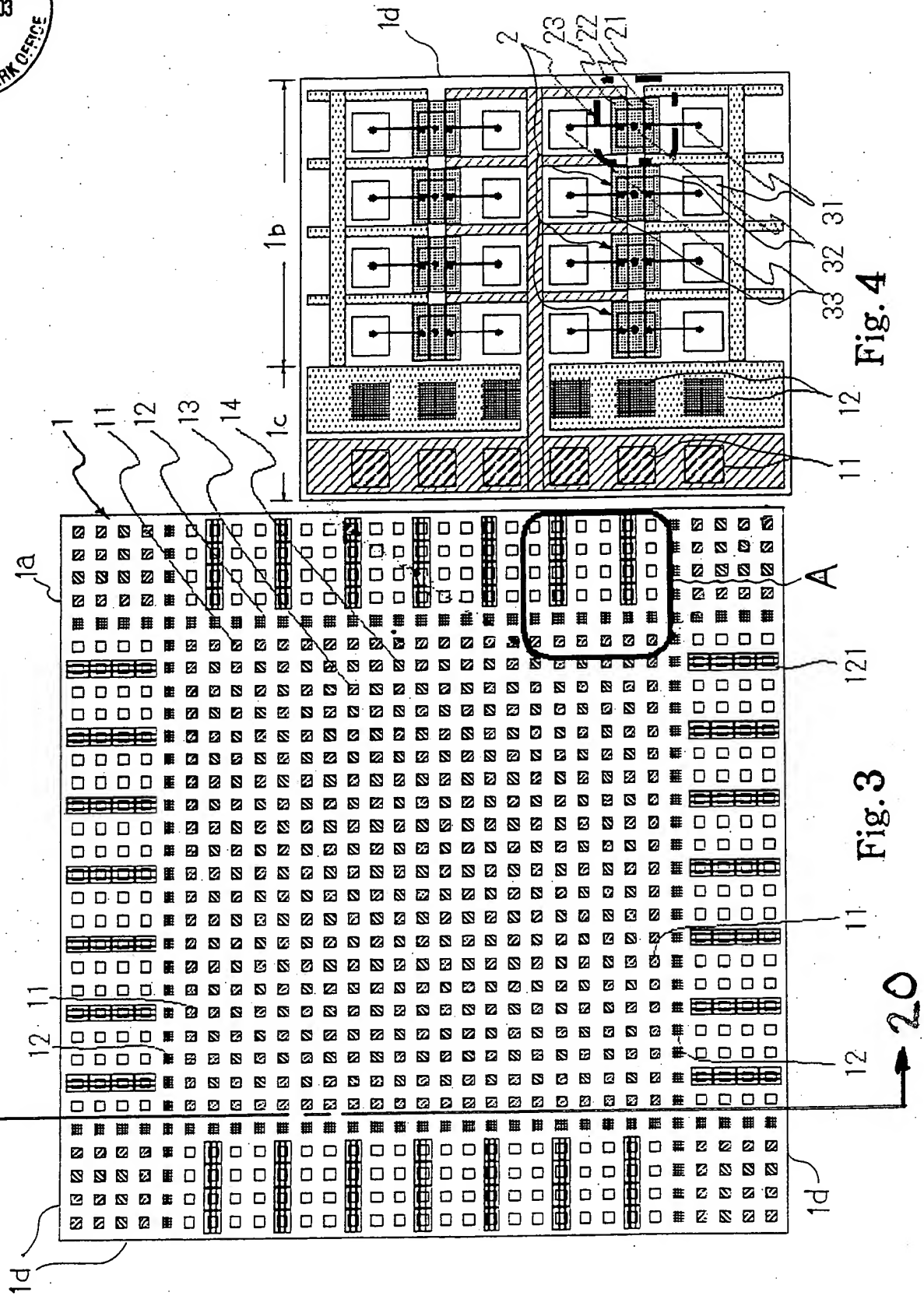

Fig. 4

Fig. 3

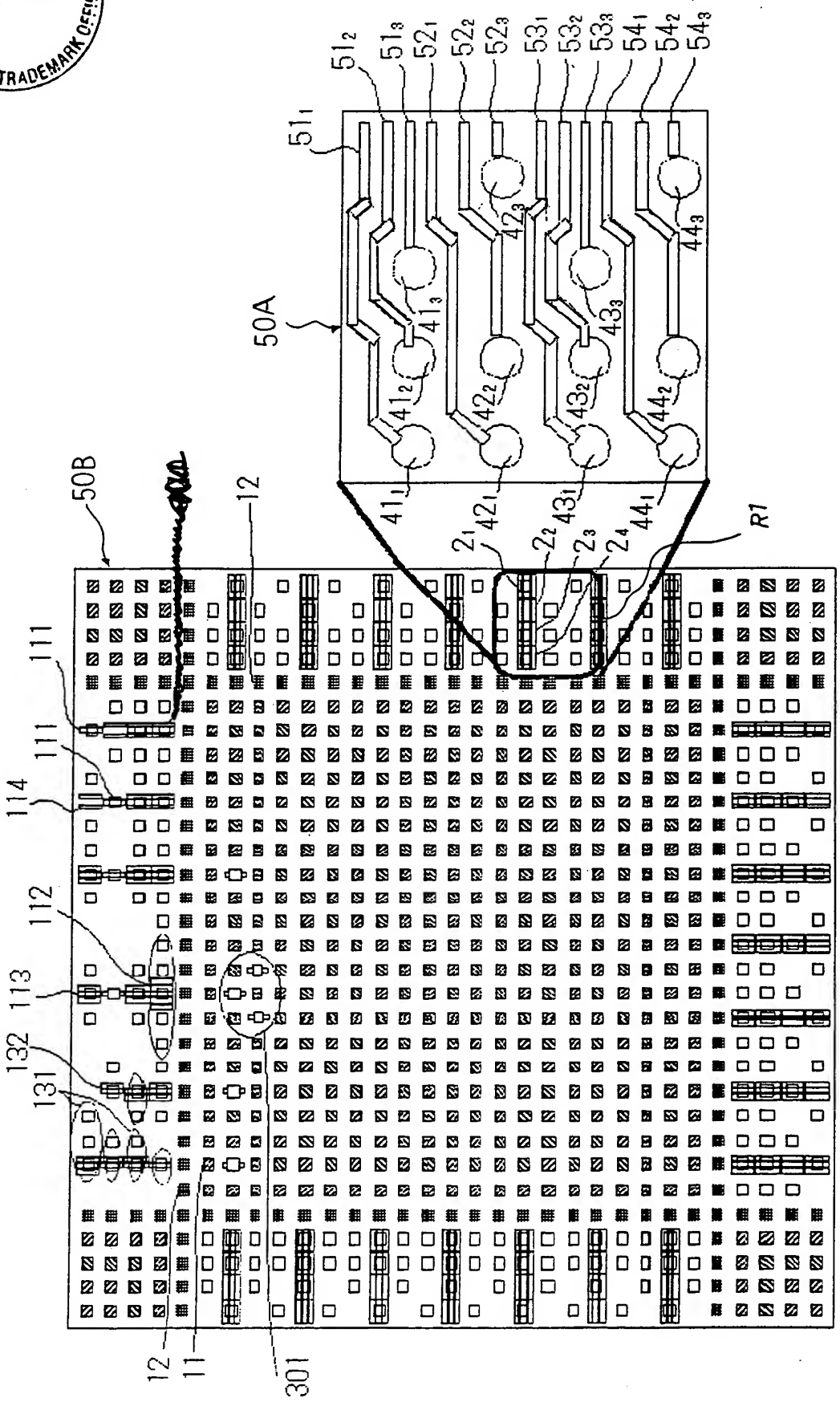

Fig. 6

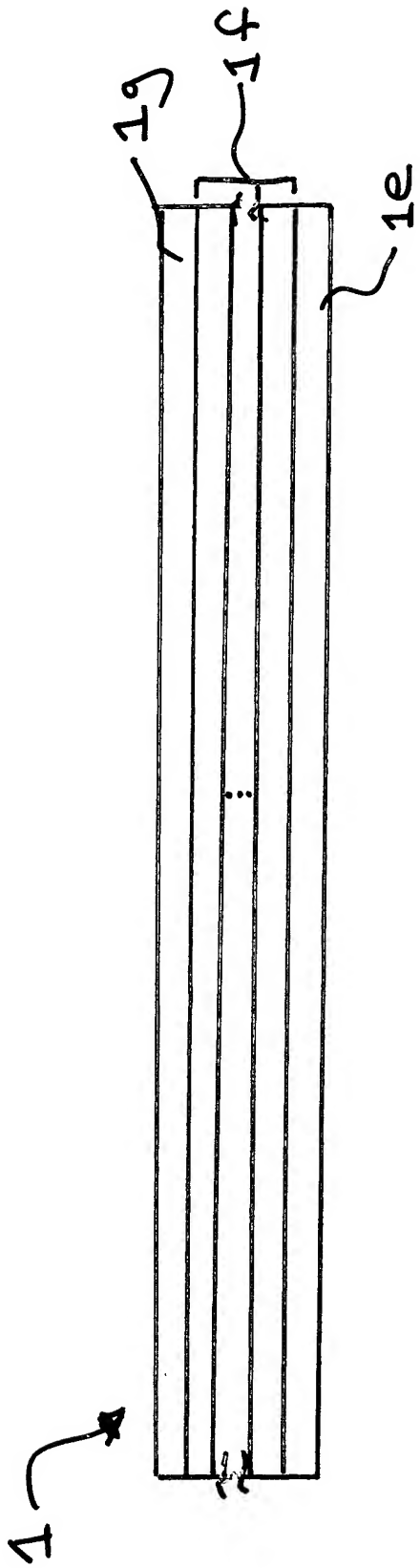

Fig. 2D

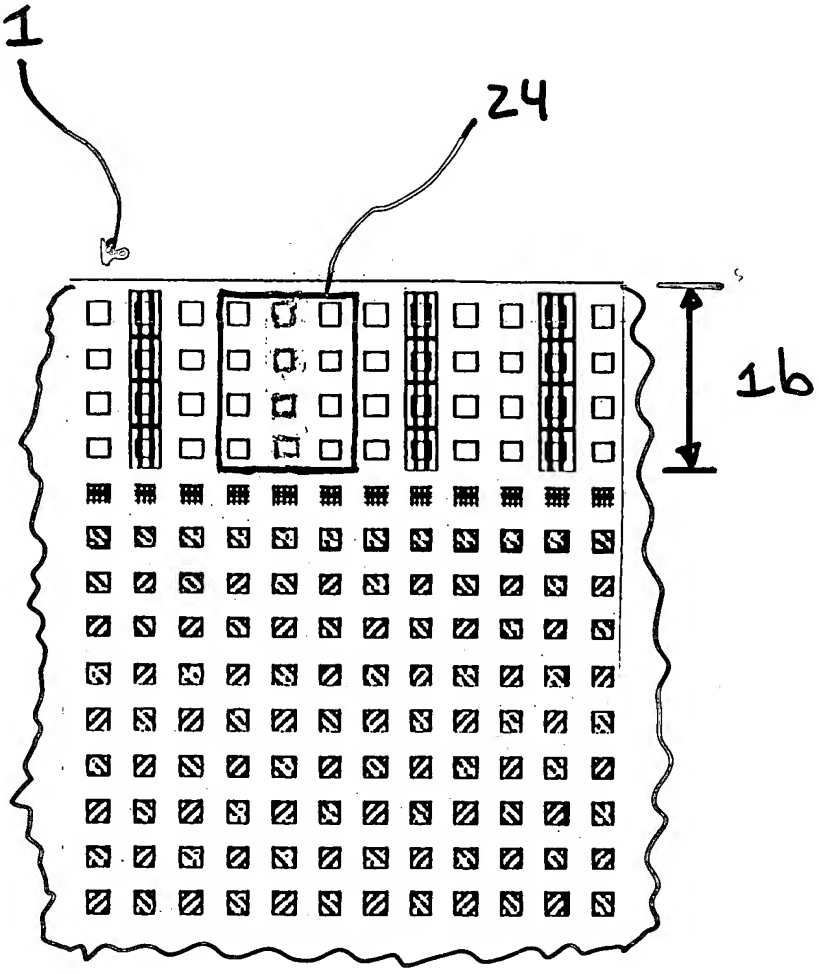

Fig. 21